Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer and including a plurality of side surfaces and a top surface;

a first gate formed on the insulating layer proximate to one of the plurality of side surfaces of the fin;

a second gate formed on the insulating layer separate from the first gate and proximate to another one of a plurality of side surfaces of the fin;

a protective layer formed above the fin, the first gate, and the second gate; and

a third gate formed over the protective layer and over the fin,

wherein the first, second, and third gates are independently addressable via respective gate electrodes.

2. (original) The semiconductor device of claim 1, further including:

first and second dielectric layers formed along the plurality of side surfaces of the fin and in contact with the first and second gates, respectively.

3. (original) The semiconductor device of claim 1, wherein the protective layer is formed to a thickness of about 150 Å to 300 Å.

4. (original) The semiconductor device of claim 1, wherein the third gate is formed to a thickness of about 200 Å to 1000 Å.

5. (original) The semiconductor device of claim 1, wherein the fin comprises at least one of silicon and germanium.

6. (original) The semiconductor device of claim 1, wherein the insulating layer comprises a buried oxide layer.

7. (original) The semiconductor device of claim 1, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin.

Claims 8-15 (cancelled)

16. (currently amended) A MOSFET device comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer;

gate dielectric layers formed on side surfaces of the conductive fin;

a first gate material layer formed on the insulating layer and around the conductive fin;

a first gate electrode connected to the first gate material layer and configured to allow the first gate material to be electrically biased;

a protective layer formed over the conductive fin and the first gate material; ~~and~~

a second gate material layer formed over the protective layer and the conductive fin; and

a second gate electrode connected to the second gate material layer and configured to allow the second gate material to be electrically biased independently of the first gate material.

17. (original) The MOSFET device of claim 16, wherein the MOSFET device is a FinFET.

18. (original) The MOSFET device of claim 16, wherein the first and second gate material layers are formed of polysilicon.

19. (original) The MOSFET device of claim 16, wherein the gate dielectric layers and the conductive fin break the first gate material layer into independently addressable first and second gates of the MOSFET device.

20. (original) The MOSFET device of claim 19, wherein the second gate material forms a third independently addressable gate of the MOSFET device.

21. (new claim) A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer and including a plurality of side surfaces and a top surface;

a first control gate formed on the insulating layer proximate to one of the plurality of side surfaces of the fin;

a first gate electrode connected to the first control gate and configured to allow the first control gate to be electrically biased;

a second control gate formed on the insulating layer separate from the first control gate and proximate to another one of a plurality of side surfaces of the fin;

a second gate electrode connected to the second control gate and configured to allow the second control gate to be electrically biased separately from the first control gate;

a protective layer formed above the fin;

a third control gate formed over the protective layer and over the fin; and

a third gate electrode connected to the third control gate and configured to allow the third control gate to be electrically biased separately from the first and second control gates.